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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,640	04/25/2000	William J. Dally	2789.2001-001	9254

21005 09/05/2003

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EXAMINER

TRAN, THIEN D

ART UNIT	PAPER NUMBER
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2665

DATE MAILED: 09/05/2003

3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/557,640

Applicant(s)

DALLY ET AL.

Examiner

Thien D Tran

Art Unit

2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-26 are rejected under 35 U.S.C. 102(b) as being participated by Li et al (U.S Patent No. 6,208,183).

Regarding claims 1, 5, 14, Li discloses a GDLL 200, col.5 lines 65, (clock multiplier) comprising:

a voltage controlled delay line 220 or 222 (delay line) which provides a multiplied clock, figure 3;

a clock multiplexer 216 which applies as an input to the delay line, at respective times, the multiplied clock and a reference clock, figure 3; and

a delay adjustment circuit including a proportional phase comparator which adjusts delay in the delay line based on a phase comparison of the reference clock and of the multiplied clock. See col.4 lines 25-35.

Regarding claims 2, 3, 8, 9, 15, 16, 21, 22, Li discloses a clock multiplier in which the phase comparator has an amount of phase offset. See col.7 lines 30-40.

Regarding claims 4, 10, 17, 23, Li discloses the delay adjustment circuit that includes a combined phase comparator and charge pump. See col.7 lines 41.

Regarding claims 6, 19, Li discloses the clock multiplier further comprises a clock multiplexer which applies as an input to the delay line, at respective times, the multiplied clock and the reference clock. See col.8 lines 10-15.

Regarding claims 7, 20, Li discloses the phase comparator is a proportional phase comparator. See col.7 lines 50-60.

Regarding claims 11, 12, 24, 25, Li discloses the data multiplexing circuit being a data multiplexer. See col.8 line 9.

Regarding claims 13, 26, Li discloses a transceiver and comprising a first multiplexing circuit, which is a data multiplexer and a second data multiplexing circuit which is a data demultiplexer. See figure 3.

Regarding claim 18, Li discloses A method of communicating data comprising:
applying a delay line output to an input of the delay line to provide a multiplied clock;
comparing the phase of the multiplied clock with a reference clock;
adjusting the delay of the delay line based on the phase comparison; and
applying the multiplied clock to a data multiplexing circuit for multiplexing data on a transmission medium. See col.9 lines 5-30.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

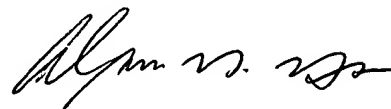
-Gaudet (US Patent No. 6,037,812) delay locked loop (DDL) based clock synthesis.

-Erickson et al (US Patent No. 5,646,564) discloses phase-locked delay loop for clock correction.

-Kurd (US Patent No. 6,043,717) discloses signal synchronization and frequency synthesis system configurable as PLL or DLL.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4388. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (703) 308-6602. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



ALPUS H. HSU
PRIMARY EXAMINER